REMARKS

Claims 1-12 are pending. By this amendment, Fig. 1 and the Specification are amended in accordance with the Examiner's recommendations. Additionally, Claim 10 has been amended to remove a reference number. Applicants respectfully request reconsideration of the rejection of Claims 1-12 under 35 U.S.C. § 102(b) in accordance with the following remarks.

Initially, Applicants would like to thank Examiners Ho and Ellis for the courtesies extended to Applicants' representative, Mr. Jason Vick, during the January 13th Personal Interview. At the interview, the general operation of the invention was discussed in relation to Fig. 2 as well as distinctions illustrated between Claim 1 and the Ekanadham reference.

The Office Action rejects Claims 1-12 under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 6,085,295 to Ekanadham (hereinafter "Ekanadham"). This rejection is respectfully traversed.

Claim 1 recites, *inter alia*, a coherence controller connected to at least one multiprocessor within a local module, said multiprocessor including a local main memory and a plurality of processors each equipped with a cache memory, said coherence controller comprising a cache filter directory including a first filter directory for guaranteeing coherence between the local main memory and the cache memory in each of the processors of the local module and a complimentary filter directory for tracking locations of lines or blocks of the local main memory copied from the local module into at least one external module and for guaranteeing coherence between the local main memory and the cache in each of the processors of the local module and at least one external module.

Claim 10 recites, *inter alia*, a local coherence controller connected to said multiprocessors and including a local cache filter directory for guaranteeing local coherence between a local main memory and the cache memories in each of said multiprocessors... wherein the coherence controller further includes a complementary cache filter directory for tracking a location of memory lines or blocks copied from said first multiprocessor module to the second one of said multiprocessor modules and for guaranteeing coherence between the local main memory and the cache memories in each of the multiprocessors in said first module and the second one of said multiprocessor.

Ekanadham at least fails to disclose or suggest the cache filter directory and complimentary filter directory as claimed. Furthermore, and as discussed during the Personal Interview, Ekanadham fails to disclose the underlying architecture that would necessitate the need to maintain coherence as outlined in the independent claims.

For example, Fig. 4 of Ekanadham discloses:

> ... the internal structure of the adapter that enables it to extend cache-coherent shared memory across multiple nodes. It comprises a set of node lists 41 and local processor lists 42. List 41 is maintained for each line of local memory that is cached at a remote node, and list 42 is maintained for each line of remote memory that is cached by a local processor. It also maintains a 2-bit line state directory 43 for lines that are cached by the local processors. The finite state machine (FSM) 40-1 and 2 runs the cache coherence protocol to keep the copies of the lines coherent. When the adapter acts as a proxy processor for a line, it uses the node list associated with the line to determine the remote nodes that need to be notified for coherence actions. When the adapter acts as a proxy memory for a line, it uses the local processor list associated with the line to determine the local processors that need to be notified for coherence actions.

Thus, it is clear that Ekanadham does not maintain coherence between the various memories as the claimed cache filter directory and complementary filter directory do. In contrast, Ekanadham discloses list 41 which is maintained for each line of local memory that

is cached at a remote node, list 42 which is maintained for each line of remote memory that is cached by a local processor and a 2-bit line state directory 43 for lines that are cached by the local processors.

Ekanadham does not anticipate the claimed invention. Furthermore, it would not have been obvious to modify the teachings of Ekanadham to achieve the exemplary benefits outlined on pages 3-5 of Applicants' Specification since Ekanadham suffers from some of the same drawbacks as highlighted in Applicants' Specification.

For at least the reasons outlined above, and the additional feature(s) recited therein, it will be appreciated that the dependent claims are also not anticipated by Ekanadham. For example, Ekanadham fails to teach or suggest the presence vector as recited in Claims 2 and 11 and the switching device and associated functionality of Claims 9 and 12. Thus, the rejection under 35 U.S.C. § 102 is untenable and should be withdrawn.

An early Notice of Allowance is respectfully requested.

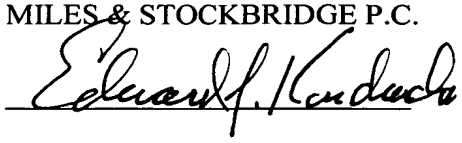
Should the Examiner believe anything further is desirable in order to place the application in even better condition for allowance, the Examiner is encouraged to contact Applicants' undersigned representative at the telephone number listed below.

The Commissioner is hereby authorized to charge to deposit account number 50-1165 (Docket No. T2147-907715) and fees not included herein, under 37 CFR §§ 1.16 and 1.17, that may be required by this paper and to credit any overpayment to that Account. A

duplicate copy of this page is included for such purpose. If any additional extension of time is required in connection with the filing of this paper and has not been separately requested, such extension is hereby requested.

Respectfully submitted,

MILES & STOCKBRIDGE P.C.



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